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10/708,786	03/25/2004	Heng-Kuan Lee	FTCP0032USA	2785

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EXAMINER	
VANCHY JR, MICHAEL J	

ART UNIT	PAPER NUMBER
2609	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/708,786	LEE, HENG-KUAN	
	Examiner	Art Unit	
	Michael Vanchy Jr.	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1 and 2 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Publication No. 2005/0238246 A1. Although the conflicting claims are not identical, they are not patentably distinct from each other because differences in scope do not rise to the level of patentable distinction.

3. Claim 16 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 9 of U.S. Publication No. 2005/0238246 A1. Although the conflicting claims are not identical, they are not patentably distinct from

each other because differences in scope do not rise to the level of patentable distinction.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 16-20, 28, 29, 33, 34, 37-39, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Finotello et al., 5,903,310.

Re claim 1, Finotello discloses a method of data coding/decoding (Figs 1-2), the method comprising: reading a data matrix (col. 6, lines 60-65), the data matrix comprising a plurality of data elements (col. 3, lines 62-67, "transform coefficients" are data elements); constructing a reference matrix based on the data matrix so that the reference matrix comprises a plurality of reference elements each corresponding to a data element (Finotello et al., col. 3, lines 32-42), each reference element representing whether its corresponding data element fits a default or not; and taking a decision step for each data element when the data matrix is written into a memory so that when a reference element corresponding to a data element represents that the data element fits the default, the data element is prevented from being written into the memory (Finotello et al., col. 11, lines 7-16).

Re claim 2, the data coding/decoding method of claim 1 further comprising: in the decision step, wherein when a reference element corresponding to a data element represents that the data element does not fit the default, the data element is written into the memory (Finotello et al., col. 11, lines 7-16).
The examiner takes into account that if the element does not fit the default, the memory will not be "disabled" and thus the data element will be written to memory.

Re claim 3, the data coding/decoding method of claim 1 further comprising: receiving an image data (Fig. 1, item "1"); generating a block based on the image data (Fig. 1, item "Q"); taking a frequency-domain transformation to the block for generating an output data; and generating the data matrix based on the output data (Finotello et al., Fig. 1, item "T", col. 3, lines 63-65, and col. 7, lines 58-67).

Re claim 4, the data coding/decoding method of claim 3 wherein the frequency-domain transformation is a two-dimensional discrete cosine transformation (Finotello et al., col. 3, lines 63-66).

Re claim 5, the data coding/decoding method of claim 3 wherein when output data based on the frequency domain transformation generates the data matrix, the data matrix is generated by quantizing the output data (Finotello et al., Fig. 1, item "2", col. 3, lines 63-67).

Re claim 16, a processing circuit for data coding/decoding comprising (Finotello et al., Abstract): a memory capable of storing a data matrix wherein the data matrix comprises a plurality of data elements; a register module for storing a reference matrix (Finotello et al., col. 7 lines 44-57) wherein the reference matrix comprises a plurality of reference elements each corresponding to a data element (Finotello et al., col. 3, lines 32-42), each reference element for representing whether its corresponding data element fits a default or not; and a decision module, wherein when the data matrix is written into the memory by the processing circuit, the decision module is capable of checking each data element so that when a reference element corresponding to a data element represents that the data element fits the default, the data element is prevented from being written into the memory (Finotello et al., col. 11, lines 7-16).

Re claim 17, the processing circuit (Finotello et al., Abstract) of claim 16 wherein when the decision module takes a decision, the data element is written into the memory if the reference element corresponding to a data element represents that the data element does not fit the default (Finotello et al., col. 11, lines 7-16).
The examiner takes into account that if the element does not fit the default, the memory will not be "disabled" and thus the data element will be written to memory.

Re claim 18, the processing circuit (Finotello et al., Abstract) of claim 16 further comprising: a frequency-domain transformation module for processing a frequency-

domain transformation to a block for generating an output data (Finotello et al., col. 3, lines 63-65, and col. 7, lines 58-67); and a quantization module for generating the data matrix based on the output data (Finotello et al., col. 3, lines 63-67).

Re claim 19, the processing circuit (Finotello et al., Abstract) of claim 18 wherein the frequency-domain transformation is a two-dimensional discrete cosine transformation (Finotello et al., col. 3, lines 63-66).

Re claim 20, the processing circuit (Finotello et al., Abstract) of claim 18 wherein the quantization module generates the data matrix by quantizing the output data (Finotello et al., col. 3, lines 63-67).

Re claim 28, a processing circuit for data coding/decoding comprising (Finotello et al., Abstract): a memory for storing a data matrix wherein the data matrix comprises a plurality of data elements; a register module for storing a reference matrix (Finotello et al., col. 7 lines 44-57), the reference matrix comprising a plurality of reference elements each corresponding to a data element (Finotello et al., col. 3, lines 32-42), each reference element for representing whether its corresponding data element fits a default or not; and a decision module, wherein when the data matrix is written into the memory by the processing circuit, the decision module is capable of processing a checking step based on each reference element of the reference matrix so that when a reference element corresponding to a data element represents that the data element fits the

default, the data element is not written into the memory (Finotello et al., col. 11, lines 7-16).

Re claim 29, the processing circuit (Finotello et al., Abstract) of claim 28 wherein when the decision module processes a decision, the data element is written into the memory if the reference element corresponding to a data element represents that the data element does not fit the default (Finotello et al., col. 11, lines 7-16).

Re claim 33, a data coding/decoding method comprising: reading a frequency-domain matrix (Finotello et al., col. 7 line 58 to col. 8 line 4), the frequency-domain matrix comprising a plurality of frequency-domain elements; providing a reference matrix comprising a plurality of reference elements each corresponding to a frequency-domain element (Finotello et al., col. 3, lines 32-42), each reference element representing whether its corresponding frequency-domain element fits a default or not; and taking a transformation step for generating an output matrix based on the frequency-domain matrix, the transformation step comprising: taking a transformation checking step for checking if the reference matrix fits a default matrix; if the reference matrix does not fit the default matrix, a corresponding output matrix is generated by proceeding to a transformation operation for the frequency-domain matrix; and if the reference matrix fits the default matrix, the frequency-domain matrix is prevented from undergoing the transformation operation and the output matrix is a constant matrix (Finotello et al., col. 3 lines 32-36, lines 59-66).

Re claim 34, the data coding/decoding method of claim 33 wherein at least one frequency-domain element is a direct current frequency-domain element and other frequency elements are alternating current frequency-domain elements among the plurality of frequency-domain elements; wherein when the reference matrix fits the default matrix, each reference element corresponding to each alternating current frequency-domain element in the reference matrix represents that the alternating current frequency-domain element fits the default (Finotello et al., col. 3 lines 32-36, line 59 to col. 4 line 4).

In Finotello et al., the discrete cosine transform macro-block inherently comprises a DC element and AC elements.

Re claim 37, the data coding/decoding method of claim 33 wherein the transformation operation is an inverse discrete cosine transformation (Finotello et al., col. 4 lines 8-10).

Re claim 38, a processing circuit (Finotello et al., Abstract) for data coding/decoding comprising: a memory capable of storing a frequency-domain matrix, the frequency-domain matrix (Finotello et al., col. 7 line 58 to col. 8 line 4) comprising a plurality of data elements; a register module for storing a reference matrix (Finotello et al., col. 7 lines 44-57) wherein the reference matrix comprises a plurality of reference elements each corresponding to a frequency-domain element, each reference element

for representing whether its corresponding frequency-domain element fits a default or not; and a transformation module (Fig. 1, item "T") for providing a corresponding output matrix based on the frequency-domain matrix, the transformation module comprising: a transformation operation module; and a transformation checking module for checking if the reference matrix fits a default matrix; wherein if the reference matrix does not fit the default matrix, the transformation checking module triggers the transformation operation module to proceed to a transformation operation for generating a corresponding output matrix, and if the reference matrix fits the default matrix, the transformation checking module is prevented from triggering the transformation operation module to proceed to the transformation operation for generating a corresponding output matrix and the output matrix is a constant matrix (Finotello et al., col. 3 lines 32-36, lines 59-66).

Re claim 39, a processing circuit (Finotello et al., Abstract) for data coding/decoding of claim 38 wherein at least one frequency-domain element is a direct current frequency-domain element and other frequency elements are alternating current frequency-domain elements among the plurality of frequency-domain elements; wherein when the reference matrix fits the default matrix, each reference element corresponding to each alternating current frequency-domain element in the reference matrix represents that the alternating current frequency-domain element fits the default (Finotello et al., col. 3 lines 32-36, line 59 to col. 4 line 4).

In Finotello et al., the discrete cosine transform macro-block inherently comprises a DC element and AC elements.

Re claim 42, the processing circuit (Finotello et al., Abstract) for data coding/decoding of claim 38 wherein the transformation operation module is capable of performing an inverse discrete cosine transformation (Finotello et al., col. 4 lines 8-10).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 6-7, 12-13, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finotello et al., 5,903,310 as applied to claim 1 above, and further in view of Kondo et al., 5,781,242.

Finotello et al. teaches about preventing data to be written to memory but is silent on preventing reading from memory. However, Kondo et al. teaches of being able to

prevent access from writing and reading to and from memory. Thus, even though Finotello et al. is silent on preventing from reading from memory, Kondo et al. teaches that both can be accomplished.

Re claim 6, the data coding/decoding method of claim 1 further comprising: taking a second decision step for each reference element when a data matrix stored in the memory is read so that the memory is prevented from being read when a reference element corresponding to a data element represents that the data element fits the default (Kondo et al., Abstract and Fig. 10 item 18 and col. 10 line 63 to col. 11 line 27).

Re claim 7, the data coding/decoding method of claim 6 further comprising: in the second decision step, wherein if a reference element corresponding to a data element represents that the data element does not fit the default, the data element is read from the memory (Kondo et al., Abstract and Fig. 10 item 18 and col. 12 lines 7-13).

Re claim 12, a data coding/decoding method comprising: reading a reference matrix before reading a data matrix from a memory, wherein the reference matrix comprises a plurality of reference elements each corresponding to a data element of the data matrix (Finotello et al., col. 3, lines 32-42), each reference element representing whether its corresponding data element fits a default or not; and taking a decision step for each reference element of the reference matrix when the data matrix is read from

the memory so that the memory is prevented from being read when a reference element corresponding to a data element represents that the data element fits the default (Kondo et al., Abstract and Fig. 10 item 18 and col. 10 line 63 to col. 11 line 27).

Re claim 13, the data coding/decoding method of claim 12 further comprising: in the decision step, when a reference element corresponding to a data element represents that the data element does not fit the default, the data element is read from the memory (Kondo et al., Abstract and Fig. 10 item 18 and col. 12 lines 7-13).

Re claim 21, the processing circuit (Finotello et al., Abstract) of claim 16 wherein when the processing circuit reads a data matrix stored in the memory, the decision module is capable of taking a further decision for each reference element so that when a reference element corresponding to a data element represents that the data element fits the default, the processing circuit (Finotello et al., Abstract) is prevented from reading the data element from the memory (Kondo et al., Abstract and Fig. 10 item 18 and col. 10 line 63 to col. 11 line 27).

Re claim 22, the processing circuit (Finotello et al., Abstract) of claim 21 wherein when the processing circuit reads a data matrix stored in the memory, the data element is permitted to be read from the memory by the decision module if the reference element corresponding to a data element represents that the data element does not fit the default (Kondo et al., Abstract and Fig. 10 item 18 and col. 12 lines 7-13).

6. Claims 8-9, 14-15, 23-24, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finotello et al., 5,903,310 and Kondo et al., 5,781,242 as applied to claim 6 above, and further in view of Yocom, 2004/0083227.

Finotello et al. and Kondo et al., teach ways of reducing the access of memory, but they both are silent on a checking step. However, Yocom does teach about a memory efficient matrix, which does checking to see if the matrix is an empty set and if so ends.

Re claim 8, the data coding/decoding method of claim 6 further comprising: after a reference element undergoes the second decision step, each reference element not yet undergoing the second decision step undergoes a checking step for checking if there is another reference element representing that its corresponding data element does not fit the default (Yocom, [0051]).

Therefore, taking the combined teachings of Finotello et al., Kondo et al., and Yocom as a whole, it would have been obvious to add a checking step.

Re claim 9, the data coding/decoding method of claim 8 further comprising: in the checking step, if all reference elements not yet undergoing the second decision step represent that their corresponding data elements fit the default, reading of the data matrix is stopped (Kondo et al., col. 11 lines 23-27).

Re claim 14, the data coding/decoding method of claim 12 further comprising: after each reference element undergoes the decision step, a checking step is taken for each reference element not yet undergoing the decision step for checking if there is another reference element representing that its corresponding data element does not fit the default (Yocom, [0051]).

Re claim 15, the data coding/decoding method of claim 14 further comprising: in the checking step, wherein if any reference element corresponding to a data element not yet undergoing the decision step represents that the data element fits the default, reading of the data matrix is stopped (Kondo et al., col. 11 lines 23-27).

Re claim 23, the processing circuit (Finotello et al., Abstract) of claim 21 further comprising: a checking module, wherein after the decision module processes decisions for each reference element, the checking module is capable of processing a further checking step for each reference element without taking the further decision for checking if there is another reference element representing that its corresponding data element does not fit the default (Yocom, [0051]).

Re claim 24, the processing circuit (Finotello et al., Abstract) of claim 23 wherein after the checking module proceeds with checks, the processing circuit reading the data matrix is stopped by the checking module if all reference elements not undergoing the

decision represent that their corresponding data elements fit the default (Kondo et al., col. 11 lines 23-27).

Re claim 31, the processing circuit (Finotello et al., Abstract) of claim 30 wherein after the checking module processes checks, the processing circuit reading the data matrix is stopped by the checking module if all reference elements not yet undergoing the decision represent that their corresponding data elements fit the default (Kondo et al., col. 11 lines 23-27).

7. Claim 11, 25, 30, 35, 36, 40, 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finotello et al., 5,903,310 as applied to claim 1 above, and further in view of Yocom, 2004/0083227.

Finotello et al. is silent about using null as the default. However Yocom does:

Re claim 11, the data coding/decoding method of claim 1 wherein the default is null (Yocom, [0039]).

Therefore, taking the combined teachings of Finotello et al. and Yocom as a whole, it would have been obvious to use null as the default.

Re claim 25, the processing circuit (Finotello et al., Abstract) of claim 16 wherein the default is null (Yocom, [0039]).

Re claim 30, the processing circuit (Finotello et al., Abstract) of claim 28 further comprising: a checking module, wherein after the decision module processes decisions for each reference element, the checking module is capable of processing a further checking step for each reference element not yet undergoing the decision of the decision module for checking if there is another reference element representing that its corresponding data element does not fit the default (Yocom, [0051]).

Re claim 35, the data coding/decoding method of claim 34 further comprising: when the reference matrix fits the default matrix (Yocom, [0039]), a constant operation step is performed for generating the constant matrix by working out a constant value based on the direct current frequency-domain element so that a plurality of elements of the constant matrix equal the constant value (Finotello et al., col. 4 lines 8-10).

Although "constant" is not expressly disclosed per se, the examiner takes into account that the default matrix can be a null matrix and thus go through an "inverse transform" obvious to the examiner to result in a matrix with elements that have a constant value.

Re claim 36, the data coding/decoding method of claim 33 wherein the default is null (Yocom, [0039]).

Re claim 40, the processing circuit (Finotello et al., Abstract) for data coding/decoding of claim 39 further comprising: a constant operation module; wherein

when the reference matrix fits the default matrix (Yocom, [0039]), the transformation checking module triggers the constant operation module to generate a constant value and the constant matrix based on the direct current frequency-domain element so that a plurality of elements of the constant matrix equal the constant value (Finotello et al., col. 4 lines 8-10).

Although "constant" is not expressly disclosed per se, the examiner takes into account that the default matrix can be a null matrix and thus go through an "inverse transform" obvious to the examiner to result in a matrix with elements that have a constant value.

Re claim 41, the processing circuit (Finotello et al., Abstract) for data coding/decoding of claim 38 wherein the default is null (Yocom, [0039]).

8. Claim 10, 26, 27, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finotello et al., 5,903,310 as applied to claim 1 above, and further in view of Mitchell et al., 4,888,645.

Finotello et al. is silent about the size of the reference element data. However, Mitchell teaches the use of one-bit data representation.

Re claim 10, the data coding/decoding method of claim 1 wherein each reference element is a one-bit data for representing whether its corresponding data fits the default or not (Mitchell et al. col. 2 lines 31-41).

Therefore, taking the combined teachings of Finotello et al. and Mitchell et al. as a whole, it would have been obvious to use a one-bit data for a reference element.

Re claim 26, the processing circuit (Finotello et al., Abstract) of claim 16 wherein the register module is a shift keying register (Mitchell et al. col. 7 lines 3-29), and each reference element is a one-bit data for representing whether its corresponding data element fits the default or not (Mitchell et al. col. 2 lines 31-41).

Re claim 27, the processing circuit (Finotello et al., Abstract) of claim 26 further comprising: a shift keying control module, wherein when the processing circuit reads the data element from the data matrix by a default sequence, the shift keying control module controls shift keying of the register module sequentially by the default sequence so that the decision module is capable of checking each reference element corresponding to each data element sequentially (Mitchell et al. col. 7 lines 3-29).

Re claim 32, the processing circuit (Finotello et al., Abstract) of claim 28 further comprising: a shift keying control module, wherein when the processing circuit reads the data element of the data matrix by a default sequence, the shift keying control module controls shift keying of the register module sequentially by the default sequence so that the decision module is capable of checking each reference element corresponding to each data element sequentially (Mitchell et al. col. 7 lines 3-29).

Examiner's Note

The referenced citations made in the rejection(s) above are intended to exemplify areas in the prior art document(s) in which the examiner believed are the most relevant to the claimed subject matter. However, it is incumbent upon the applicant to analyze the prior art document(s) in its/their entirety since other areas of the document(s) may be relied upon at a later time to substantiate examiner's rationale of record. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). However, "the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Vanchy Jr. whose telephone number is (571) 270-1193. The examiner can normally be reached on Monday - Friday 7:30 am - 5:00 pm Alt. Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on (571) 272-7332. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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